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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,614	03/16/2004	Deok-Hyung Lee	5649-1272	2903

7590 06/07/2005

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EXAMINER	
DICKEY, THOMAS L	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,614	LEE ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/16/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 04/01/05 has been entered.

Election/Restriction

2. Applicant's election without traverse of Group II, claims 1-7 and 13-20, in the Paper filed 04/01/05 is acknowledged.

Oath/Declaration

3. The oath/declaration filed on 01/02/98 is acceptable.

Drawings

4. The formal drawings filed on 3/16/2004 are acceptable.

Priority

5. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

6. The Information Disclosure Statement filed on 3/16/2004 has been considered.

Claim Objections

7. Claim 6 is objected to because of the following informalities:

Claim 6 gives the appearance of lacking proper antecedent basis for "the second layer." It is assumed Applicants intended claim 6 to depend from claim 2, which introduces "a second layer." Claim 6 will be examined under the assumption that it properly depends from claim 2.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8 and 13-18 are rejected under 35 U.S.C. 102(b) as being anticipated by INABA ET AL. (6,525,403).

With regard to claims 1-7, Inaba et al. discloses a field effect transistor with a substrate 11-12 including a semiconductor layer 11 and an insulation layer 12 on the semiconductor layer 11; a fin 11A-15-16-21 on the insulation layer 12 and extending from the substrate 11-12, the fin 11A-15-16-21 including a first layer 21 in an upper portion remote from the substrate 11-12 and sidewalls that extend between the upper portion and

the substrate 11-12; a second layer 11A beneath the first layer 21; a channel region in the fin 11A-15-16-21; a gate electrode 14 adjacent the channel region-and crossing over the fin 11A-15-16-21; a gate insulation layer 13 interposed between the gate electrode 14 and the fin 11A-15-16-21; and source/drain regions formed at both sides of the gate electrode 14, wherein the second layer 11A is lightly doped relative to the first layer 21, so that the channel region at the upper portion of the fin 11A-15-16-21 is doped higher than sidewalls of the fin 11A-15-16-21, wherein the substrate 11-12 is a bulk semiconductor layer 11; and wherein the semiconductor layer 11 extends vertically to form the fin 11A-15-16-21; wherein the insulation layer 12 is disposed between the gate electrode 14 and the semiconductor layer 11 at a periphery of the fin 11A-15-16-21 and the second layer 11A has uniform concentration in the channel region; and further comprising a punch-through stop layer 17 beneath the channel region having a higher doping concentration than the second layer 11A. Note figure 7 and column 7 lines 1-30 of Inaba et al.

With regard to claims 13-18, Inaba et al. discloses a field effect transistor with an integrated circuit substrate 11-12 comprising an insulating layer 12 on a substrate 11; a fin 11A-15-16-21 on the insulating layer 12, opposite the substrate 11, that projects away from the integrated circuit substrate 11-12, extends along the integrated circuit substrate 11-12 and includes a top that is remote from the integrated circuit substrate 11-12; a channel region 11A-21 in the fin 11A-15-16-21 comprising a first region 21 of the predetermined conductivity type adjacent the top, and a second region 11A of the

predetermined conductivity type remote from the top, wherein the first region 21 is more heavily doped than the second region 11A, so that the channel region 11A-21 is doped a predetermined conductivity type and has a higher doping concentration of the predetermined conductivity type adjacent the top than remote from the top, and thus is uniformly doped the predetermined conductivity type at a first doping concentration except for being doped the predetermined conductivity type at a second doping concentration that is higher than the first doping concentration adjacent the top wherein the fin 11A-15-16-21 includes first and second sidewalls that extend between the top and the substrate 11 and wherein the channel region 11A-21 has the higher doping concentration of the predetermined conductivity type directly beneath the top, from the first sidewall to the second sidewall; a source region 15 and a drain region 16 in the fin 11A-15-16-21 on respective opposite sides of the channel region 11A-21; and an insulated gate electrode 14 that extends across the fin 11A-15-16-21, adjacent the channel region 11A-21, wherein the integrated circuit substrate 11-12 is a bulk semiconductor substrate 11 such that the bulk semiconductor substrate 11 includes a projection that defines the fin 11A-15-16-21; the integrated circuit field effect transistor further comprising a region 17 of the predetermined conductivity type in the bulk semiconductor substrate 11 beneath the fin 11A-15-16-21. Note figure 7 and column 7 lines 1-30 of Inaba et al.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 13,19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over BROWN ET AL. (2004/0126969) in view of INABA ET AL. (6,525,403).

Brown et al. discloses an integrated circuit field effect transistor with an integrated circuit substrate 10'; a fin 12A that projects away from the integrated circuit substrate 10', extends along the integrated circuit substrate 10' and includes a top that is remote from the integrated circuit substrate 10'; a channel region in the fin 12A that is doped (note paragraph 31) a predetermined conductivity type; a source region and a capacitor connected to the source region (source and capacitors being described in paragraph 26); a drain region connected to a bit line (drain and bit lines being described in paragraph 25) in the fin 12A on respective opposite sides of the channel region; and an insulated gate electrode (note paragraphs 32-33) that extends across the fin 12A, adjacent the channel region. Note figures 2-7 and paragraphs 25-33 of Brown et al. Brown et al. does not disclose that the channel region has a higher doping concentration of the predetermined conductivity type adjacent the top than remote from the top.

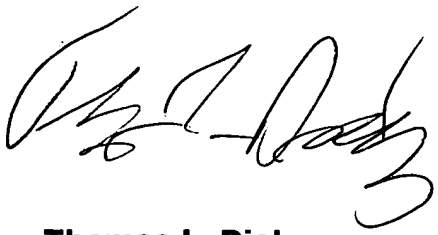
However, Inaba et al. discloses an integrated circuit field effect transistor comprising a channel region having a higher doping concentration (the P+ region identified as part 21) of the predetermined conductivity type adjacent the top than remote (the remote part of the channel has part #11a) from the top. Note figure 7 and column 7 lines 1-30 of Inaba et al. Inaba et al. explain that P+ region 21 prevents the channel from being formed in the top surface of the substrate projection, i.e., requires only the side surfaces of the fin to be used as the channel. This prevents the occurrence of punch-through between source and drain even with a very fine (i.e., short channel) gate electrode. Unlike the prior art (Inaba et al. agree with Applicants that Mizuno et al. 5,844,278 is characteristic of the prior art, compare page 2 lines 1-12 of the instant application to figures 4 and 5 and paragraph 17 of Inaba et al.), the semiconductor device according to the figure 7 embodiment of the Inaba et al.'s invention is basically characterized in that the top portion of the substrate projection is not used as the channel. Therefore, it would have been obvious to a person having skill in the art to augment Brown et al.'s a integrated circuit field effect transistor with the channel region having a higher doping concentration of the predetermined conductivity type adjacent the top than remote from the top such as taught by Inaba et al. in order to require only the side surfaces of the fin to be used as the channel to thus prevent the occurrence of punch-through between source and drain even with a short channel gate electrode.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Patent Examiner
Art Unit 2826
05/05